

The IMPACT Common Module – A Low Cost, Reconfigurable Building Block for Next Generation Phased Arrays

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Abstract: *This paper discusses the progress of this team's project known as IMPACT (Integrated Multi-use Phased Array Common Tile), which addresses a major goal of the DARPA Arrays at Commercial Timescales (ACT) program. The goal of this program has been to develop a common technology base for Electronically Scanned Array (ESA) systems. Historically, most fielded ESA systems have been comprised of highly tailored, application-specific layers. This has led to slow design cycles, costly components, and significant portions of the total cost of ownership being invested in the up-front Non-Recurring Expenses (NRE). The results section highlights the receiver side of our progress.*

Introduction

Electronically Scanned Array (ESA) systems [1-3] have many advantages over mechanically scanned designs; these include: multiple simultaneous beams, adaptive array processing, rapid inertia-less beamsteering, multi-function (i.e., both communications and radar functions), etc. Although their performance is being characterized by the research community, these ESAs, and most of their sub-components, have been application-tailored for a specific need set, volume-based pricing models have not been able to be leveraged to reduce recurring material costs. Furthermore, with each new emerging threat, long re-design cycles have been required, often demanding the entire system be re-designed. All of these factors have combined to make ESAs in today's Department of Defense (DoD) niche systems only within reach of platforms that have no choice but to make use of them (e.g. fire control radars for fighters, ground based missile defense radars, maritime missile and air defense). The cost of development and recurring cost of the hardware has placed them largely out of reach for higher volume, mobile platforms.

Modern "digitized subarray" phased arrays employ phase shifters and variable gain amplifiers at every element with a transceiver at each subarray; thus providing increasing functionality and performance at reduced cost, size, and weight compared to their predecessors [4-6]. This has been accompanied by advances in efficient front-end circuitry, improvements in packaging and integration, and an increased role of digital electronics closer to the aperture itself [7,8].

In this modern architecture, Tx/Rx beamforming is accomplished with analog combiner networks (usually passive) and phase shifters within each subarray to approximate true time delays. Digital transceivers drive the combined input/output signals of each subarray, in turn connecting to digital beamformers that operate at the sub-array level. Digitization of multiple subarray channels enables adaptive beamforming [9,10], space-time adaptive processing (STAP) [11], and multiple concurrent functions, an important requirement for future systems like the Multifunction Phased Array Radar (MPAR) [12,13].

As shown in Figure 1, the Rockwell Collins-led team on ACT, including the University of Oklahoma and Stanford University, is developing IMPACT (Integrated Multi-Use Phased Array Common Tile), a core building block on which future ESA systems can be built [14]. The core strategy we employ involves migrating ESAs towards a fundamentally digital architecture, enabled by reconfigurable RF components. As a result, RF beamformers, down-converters, digitizers, equalizers, and some of the T/R module functionality must all be located within the Common Module to enable a more flexible FPGA-based digital backbone for the array.



Figure 1. IMPACT Common Module

This highly flexible architecture is composed of digitally reconfigurable components (Figure 2). Rockwell Collins is designing the SiGe receiver and transmitter functions. The SiGe receiver has two stages of programmable RF filtering and one stage of IF filtering. Each filter can be tuned in center frequency and bandwidth and is capable of bandpass or notch topologies. Analog beamforming is employed on

transmit, with an IF to RF upconversion chain that is split to programmable phase shifters and VGAs at each output port.

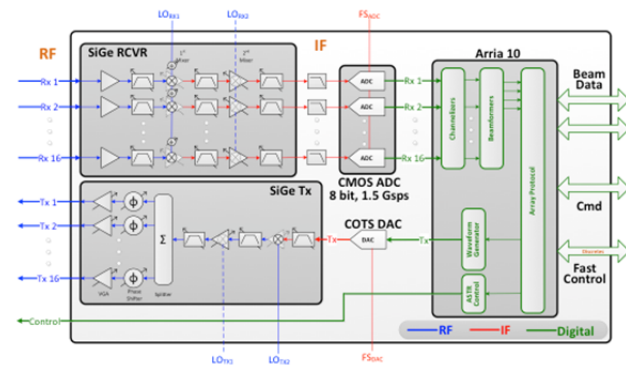


Figure 2. IMPACT Block Diagram

Analog to Digital Conversion

Stanford University is providing an 8 bit analog-to-digital converter (ADC) capable of sampling at 1.5GHz (Figure 3). The ADC consumes 10-20 times less power than currently available commercial-off-the-shelf (COTS) ADCs. This is critical for highly dense groupings of components in modern phased arrays. The target system calls for wideband IF digitization of spectral components up to 3 GHz, with a spurious free dynamic range (SFDR) greater than 60 dB. While there exist commercial parts that meet this specification, their power dissipation is on the order of Watts (see e.g. [15]), which is far too high for our application. We address this issue by creating an application-tailored design that leverages the strengths of fine-line CMOS technology (65 nm) and employs the latest innovations from the data converter research community. To achieve the aggregate conversion rate of 1.5 GS/s, the design employs four time-interleaved successive approximation register (SAR) sub-ADCs. Each slice, running at 375 MS/s, dissipates 5.9 mW, leading to a total ADC core power of only 23.6 mW. This power level is explained by the fact that the circuit contains no linear gain elements and instead relies only on switches, capacitors and latches, which capitalize on the strengths of modern CMOS.

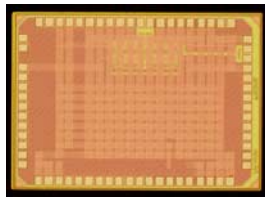


Figure 3. 1.5 Gsps, 8-Bit ADC Die

The most critical part of our ADC design is the converter front-end, which is ultimately responsible for acquiring high fidelity samples at IF frequencies. To achieve the design specs, a carefully crafted interface that considers package parasitics, finite drive impedance, and charge kick-back effects is required. The most important component in the front-end is the input buffer, whose main task is to shield the

external driver circuitry from nonlinear charge kickback (caused by the global track-and-hold (T/H) block, see Figure 4). The kickback would otherwise be very difficult to absorb by the ADC driver and would also cause ringing in the bond wire inductances.

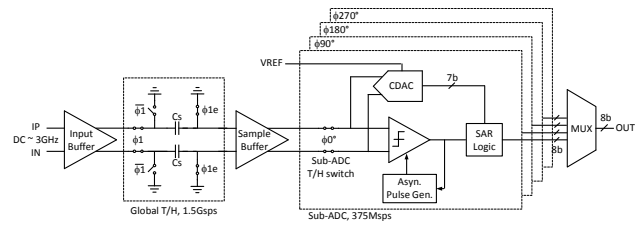


Figure 4. Stanford ADC Architecture

The input buffer is implemented using CMOS source followers and the bias currents are judiciously chosen to suppress high-frequency tracking nonlinearities well below – 60 dB. The purpose of the succeeding sample buffer is to actively drive the acquired signal onto the sampling capacitors of the SAR ADC slices. The combined power dissipation of the buffers is 36 mW and thus exceeds the power of the four-slice converter core. This is expected as the state-of-the-art ADCs designed in this spec space invest majority of power consumption in the front end to achieve high linearity. [16-17] Thus, as a research initiative we are investigating an alternative scheme in which the buffers are allowed to (weakly) distort the input signal, allowing us to save the majority of the presently invested current. The distortion is subsequently removed by additional digital processing [18], which should prove to be less power hungry than a linear-by design buffer.

Beamforming

The University of Oklahoma's *Advanced Radar Research Center* is providing expertise on digital beamforming algorithms. These are optimized to run on medium grade Field Programmable Gate Arrays (FPGAs), such as the Altera Arria 10, and represent a few of the many functions that could be implemented on the highly flexible IMPACT common module. The narrowband beamformer is highly condensed, with current designs capable of eight beamformers running simultaneously with independent pointing angle, tune frequency, and channel bandwidth. The common module will also accommodate two simultaneous wideband beamformers operating at greater than 250MHz bandwidth. Figure 5 depicts the block diagram of the narrowband beamformer.

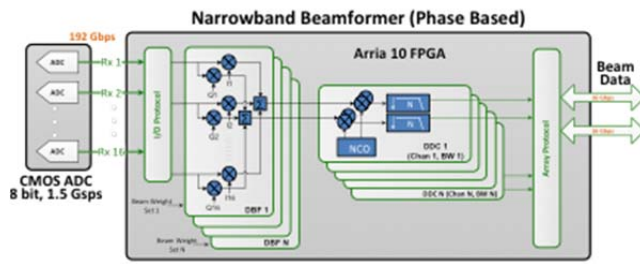


Figure 5. Narrowband Beamforming

In the narrowband beamforming architecture, the IMPACT module is configured to demonstrate a flexible receiver frontend capable of forming simultaneous narrowband beams of arbitrary channel center frequency and spacing. As given in Figure 2, the digital beamforming engine resides in the FPGA fabric and is interfaced with the superheterodyne analog frontend through sixteen ADCs. The beamformer architecture is broken into a flow of four basic stages: active register loading, beamforming and numerically controlled oscillator (NCO) generation, complex mixing, and filtering and decimation. These functions run in four polyphase branches to run at the FPGA system clock rate that is four times lower than the ADC sample rate. Beamforming weights, NCO parameters, and filter coefficients are all latched with internal registers. These are synchronized and updated over the processor interface or paired with external registers to reconfigure the system to meet the user spectral requirements and output rates. The Arria 10 design accepts data from the 16 ADCs and simultaneously processes 8 narrowband beamformers with independent point angle, NCO tune frequency, and channel bandwidth.

Figure 6 depicts the block diagram of the wideband beamformer, for which the FPGA in Figure 2 may be configured to operate. The FPGA design is currently targeted to the Altera Arria 10 10AX115NF40I3SGES device and has been compiled, tested, and verified using the System Console MATLAB API on the Attila Arria 10 instant development kit evaluation board. The purpose of the wideband beamformer is to demonstrate the instantaneous bandwidth capability, software reconfigurability, and low power operation of the IMPACT module. The wideband beamformer engine also accepts 16 channels of digital inputs and can process two independent output beams simultaneously. The design is currently fully parameterizable via a MATLAB script that configures hardware registers and software parameters simultaneously in real time. Such parameters include input and output test vectors, true time delay beamforming coefficients, calibration tables, and control variable and flags.

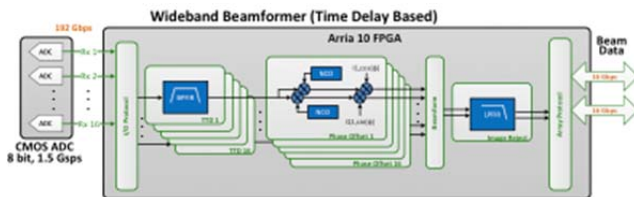


Figure 6. Wideband Beamforming

Also for current testing purposes, receive waveforms are assumed to be previously sampled by an ADC at the appropriate Nyquist sampling rate. Currently this sampling rate is configured to be 600 MHz. With a polyphasing factor of 4, the Arria 10 FPGA runs at a very conservative clock frequency of 150 MHz. Additional design work and careful constraining of the design should allow the clock speed to increase beyond 300 MHz in the future.

Using a bank of 16 FIR filters with length of 22 taps to implement true time delay beamforming, a bandwidth covering 80% of the Nyquist region can be achieved through careful design and consideration of the coefficients. More on the filter coefficient design can be found in [14]. In this case, maximum instantaneous bandwidth achievable by the IMPACT module is 240 MHz. Future builds running with an FPGA clock speed of 375 MHz will achieve a maximum instantaneous bandwidth of 600 MHz.

Resource utilization and FPGA implementation results are shown in Table 1. It should be noted that the current beamforming performance is limited by the DSP resources, which are 93% populated by the two beamforming engines. The firmware of the DSP processing core continues to be updated daily with minor iterations. Compilation time for this design can reach 2 hours on a modern desktop PC for a fully implemented design which is required for each design modification of the firmware. In essence, as design requirements change, this team can easily achieve these dynamic benchmarks with an FPGA (as opposed to an ASIC solution).

Table 1. Resource Utilization

Resource	Value
LUTs	13K/427K (3%)
BRAM	4.2Mb/55.6Mb (8%)
DSPs	1408/1518 (93%)
Power	5 W

Conclusions

The IMPACT module is a reconfigurable, common building block that will permit lower cost, quicker turn phased array developments for next generation communication, low-to-medium power radar, and wideband ELINT systems. These capabilities will provide our systems with a means to quickly and affordably respond to new threats. By architecting the device with recurring cost as a key performance parameter from the beginning, cost-neutral technology insertion of phased arrays will be possible for many systems in the DoD that currently cannot afford this technology.

Acknowledgements

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